



Networks-on-Chip: From Implementations to Programming Paradigms

By Sheng Ma, Libo Huang, Mingche Lai, Wei Shi

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Networks-on-Chip: From Implementations to Programming Paradigms provides a thorough and bottom-up exploration of the whole NoC design space in a coherent and uniform fashion, from low-level router, buffer and topology implementations, to routing and flow control schemes, to co-optimizations of NoC and high-level programming paradigms.

This textbook is intended for an advanced course on computer architecture, suitable for graduate students or senior undergrads who want to specialize in the area of computer architecture and Networks-on-Chip. It is also intended for practitioners in the industry in the area of microprocessor design, especially the many-core processor design with a network-on-chip. Graduates can learn many practical and theoretical lessons from this course, and also can be motivated to delve further into the ideas and designs proposed in this book. Industrial engineers can refer to this book to make practical tradeoffs as well. Graduates and engineers who focus on off-chip network design can also refer to this book to achieve deadlock-free routing algorithm designs.

- Provides thorough and insightful exploration of NoC design space. Description from low-level logic implementations to co-optimizations of high-level program paradigms and NoCs.
- The coherent and uniform format offers readers a clear, quick and efficient exploration of NoC design space
- Covers many novel and exciting research ideas, which encourage researchers to further delve into these topics.
- Presents both engineering and theoretical contributions. The detailed description of the router, buffer and topology implementations, comparisons and analysis are of high engineering value.

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Editorial Review

From the Back Cover

Networks-on-Chip From Implementation to Programming Paradigms Provides a thorough bottom-up exploration of NoC design

Networks-on-Chip: From Implementation to Programming Paradigms provides a thorough bottom-up exploration of the whole NoC (networks-on-chip) design space, from low-level router, buffer and topology implementations, and routing and flow control schemes, to co-optimizations of NoC and high-level programming paradigms. This textbook is intended for use in advanced courses on computer architecture, and is suitable for graduate students and senior undergraduates who want to specialize in the area of computer architecture and NoC. It is also intended for industry practitioners in the area of microprocessor design, especially the many-core processor design architecture using NoC. Those taking a course on NoC using this book, will gain both a practical and theoretical perspective, and can delve further into advanced topics by doing additional reading. Networks-on-Chip is also an excellent reference for industrial engineers looking to make practical tradeoffs. Graduates and engineers focusing on off-chip network design can also refer to this book for deadlock-free routing algorithm designs.

Key Features: Provides a thorough and insightful exploration of NoC design space, including low-level logic implementations to co-optimizations of high-level program paradigms and NoCs. Discusses many novel and exciting research ideas such as deadlock-free routing algorithm designs. Presents detailed descriptions of router, buffer, and topology implementations, that are highly valuable to engineers.

Zhiying Wang Professor Zhiying Wang is member of the IEEE and ACM, and a professor at the College of Computer, National University of Defense Technology. His main research fields include computer architecture, computer security, VLSI design, reliable architecture, multicore memory system and asynchronous circuits. He has contributed over 10 invited chapters to book volumes, published 240 papers, and delivered over 30 keynotes lectures.

About the Author

Sheng Ma received the B.S. and Ph.D. degrees in computer science and technology from the National University of Defense Technology (NUDT) in 2007 and 2012, respectively. He visited the University of Toronto from Sept. 2010 to Sept. 2012. He is currently an Assistant Professor of the College of Computer, NUDT. His research interests include on-chip networks, SIMD architectures and arithmetic unit designs.

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